Comparative Analysis among DSP and FPGA-based Control Capabilities in PWM Power Converters

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Abstract— **PWM power converters are close to be mature for standard diffusion. New FPGA technologies could now realise at best the digital control key-points: flexible performance and time to market. The paper deals with the new digital control properties of FPGA-based techniques. On the basis of reference structures, a comparative analysis is carried-out trading-off dynamic performances and immunity to PWM environment. All possible sampled control or DSP techniques are firstly analysed and compared to each other. A breakthrough concept for FPGAs is defined, definitely solving for PWM feedback immunity by practical over-sampling and parallel processing while improving dynamic performances. Simulation tests and the application of dead-beat control clearly point-out the respective dynamic properties.**

I. Introduction

Although growing-up in application for several decades, electric power conversion technologies are not still as mature as needed to define production standards. This applies particularly in PWM power applications, where electronic power modules are close to be standard products. In the field, the integration of digital control theory and technology is far from, in spite of two decades of acknowledged efforts toward standard DSP solutions.

This can be easily explained at least for medium to high power converters, where any small control improvement takes impact on the power converter cost and performance, considering as a whole power modules and filtering reactive components. As ever known, sampled digital controls cannot compare with continuous or analog control in the PWM environment.

Nowadays, thanks to novel gate-array integration levels and cost, a renewed interest is devoted to FPGAs for full integration of all control functions [1,2]. At the same time, FPGA technology is quite mature for power conversion applications, being adopted from more than one decade for the integration of glue logic and auxiliary functions.

A comparative analysis between DSP and FPGA-based control capabilities is here proposed for PWM applications, pointing-out if and how FPGAs can reach novel theoretical digital control limits for dynamic performances and rejection to peculiar PWM errors [3,4,6].

A reference control structure is adopted searching for maximum closed-loop gain values, wanted for the lowest parameter sensitivity. DSP control drawbacks in PWM converters and possible breakthrough of FPGA-based solutions are discussed. At last, the dead-beat control concept could be adopted giving comparative evidence to the intrinsic dynamic control properties.

II. Reference PWM conversion system

Proper references for both physical system and control structure are defined to compare the properties of really different control techniques. This is strictly needed for closed-loop digital control of PWM power converters, due to mutual interactions between I/Os time-sampling properties and PWM ripple effects. The current loop of Voltage-Supplied converters is here strictly considered, since any other or outer control task is much more free from those interactions.

II.A. PWM systems and parasitic effects.

State-of-the-art controlled systems are composed by current controlled Voltage-Supplied PWM power converters. A general power conversion structure is depicted in Fig. 1, indicating possible circuit models for both input voltage source and load.

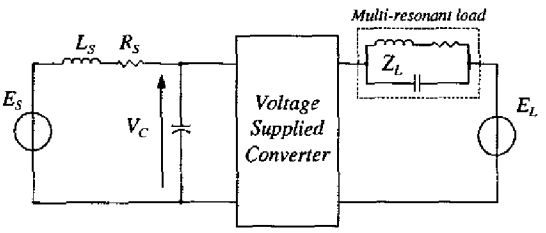

Fig. 1 Simplified sketch of simple power conversion system.

Each VS power conversion structure shows peculiar PWM voltage harmonic content, which is also variable with its operating duty cycle or modulation index.

Above the modulation frequency, the related current ripple content is depending on the load impedance. Unfortunately, the load model is hardly complex, due to different parasitic resonances and current modes.

This particularly applies in practical loads, like electric motors, where their inductance would be considered good enough for power compatibility.

This key-point must be accurately taken into account whenever current feedback time-samples are controlled.

At first, an ideal PWM system would be considered for reference. Then, any other PWM effect must be evaluated for possible rejection of unwanted related control errors.

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II.B. Reference ideal PWM converter.

The simplest PWM system, reported in Fig. 2, can be considered as the reference one for comparative evaluation of digital control techniques.

As known, the single-leg structure generates on ideal inductive load a well-defined PWM current ripple content, the reference one for sampled control loops. This is a triangular waveform since both the input voltage V_C and the load e.m.f. E_L can be assumed as constants or independent variables during some switching periods at given operating conditions.

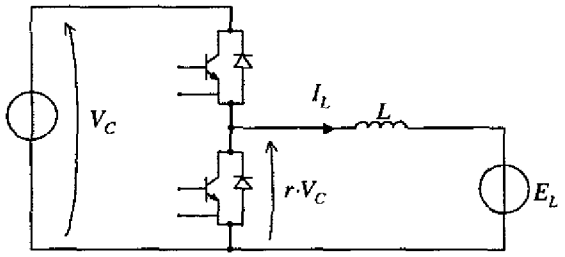

Fig. 2 Reference single-leg PWM converter and ideal source and load.

II.C. Reference control structure and concepts.

A reference control scheme is proposed in Fig. 3 according to suitable PWM properties and control concepts.

The chosen current loop regulator is a simple PI. No derivative term should be applied to feedback quantities in such a "noisy" PWM environment that is affected by load resonances. Derivative terms could apply only on reference quantities (the current I^* in the scheme). According to the proposed structure, dynamic terms may complete the feed-forward voltage load estimation or can realise the dead-beat control concept.

The proposed scheme is representing the basic concepts suitable to achieve the best performances on dynamics and reduced sensitivity to parameter errors:

- maximise the proportional gain to reduce the effects of both additive and parametric uncertainties;
- adopt accurate feed-forward compensation for additive disturbance and dynamic term estimation;
- limit integrative term span to what strictly needed to cover feed-forward estimation error, thus limiting any possible wind-up and other large signal effect.

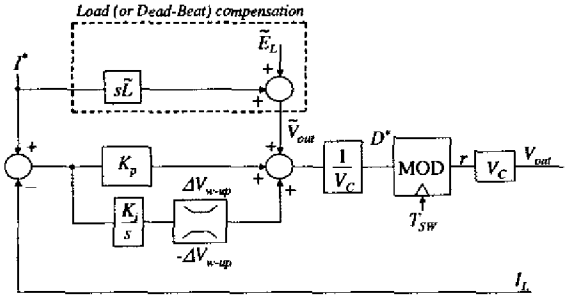

Fig. 3 PWM closed-loop current control reference structure.

III. REVIEW OF PWM SAMPLED CURRENT CONTROL

III.A. Drawbacks of sampled control loops.

Actually, to accomplish with regulation targets DSPs or microcontroller devices are commonly used to control PWM power converters. This digital environment is inherent with the adoption of feedback time-sampling strategies.

As well known, in a ideal case as that reported in Fig. 2, the feedback current samples must be kept only and exactly at the triangular PWM carrier vertexes instants: there the PWM current ripple is zero-crossing so the samples equal the wanted mean value of current.

Unfortunately, also the reference modulation index (the input of the PWM comparator) must be refreshed at the same instants, avoiding duty errors or unwanted commutations. This is why the control loop delay cannot be lower than one-half the PWM period, as the time difference between two consecutive PWM carrier vertexes.

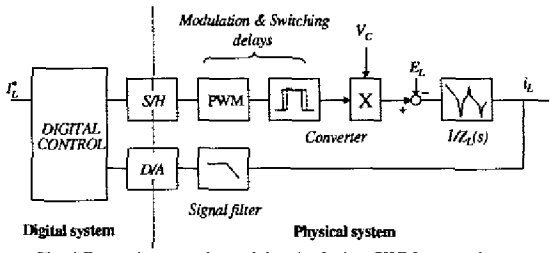

Fig. 4 Dynamic properties and drawbacks in a PWM current loop.

In addition, with reference to the block scheme in Fig. 4, other power conversion drawbacks may arise:

- the transfer signal delays and the switch commutation times imply a resultant time delay between the PWM commands and the actual switch commutations;
- different turn-off and turn-on delays are foreseen and variable with transistor temperature;
- practical dead-times in inverter legs add time-delay dependence on the sign of output current;
- the Z_L impedance is not purely inductive, resulting in a PWM current ripple zero-crossing error;
- more important, the stray resonances of Z_L (and cables) may be excited by PWM modulation harmonics, varying with duty and dramatically increasing sampling errors and their uncertainty with respect to expected mean current value.

As a requirement of all, a low-pass filter is applied in practice on the A/D current signal input, trying to reduce the related sampling errors. As a result, a further control-loop phase margin is lost.

Sketched in Fig. 5, all single current samples are kept by some delay (γ) with respect to PWM carrier vertexes, searching for the instant where the filtered PWM current ripple actually crosses zero. This is the result of all time-delays, those from PWM commands to transistor switchings and those equivalently related to A/D input filter. However it is very difficult to set the correct sample instant, dependently also on the current sign in inverter modules.

III.B. Overview of sampled control techniques.

The sketch reported in Fig. 5 summarises possible sampling instants and control techniques.

Depending on the calculation speed and clock of the microcontroller or DSP, four different combinations are possible. A comparative analysis is carried out to compare performances and drawbacks.

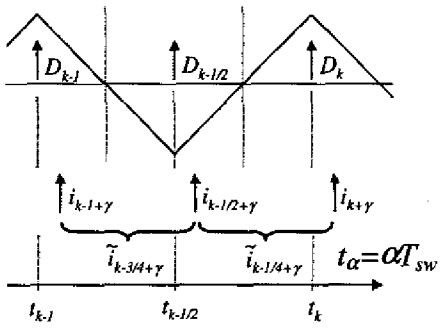

Fig. 5 Sampling techniques: A/D current samples and averaged values; modulation index output refresh instants with reference to PWM carrier.

With reference to the block scheme in Fig. 4, dynamic uncertainties, parasitic load resonances and A/D signal filter could be reported as a whole in terms of sampling error sensitivity to residual PWM ripple or equivalent "digital noise". On the other hand, the effects of such dynamic non-idealities and related sampling errors are common to all sampled control cases, thus scarcely affecting the wanted comparative analysis of dynamic properties.

An ideal closed-loop delay time "T_{del}" would be found pointing-out such comparative dynamic limits. With reference to Fig. 4, this should be dominated by the sum between the control algorithm time-delay (evaluated from input A/D samples to output S/H refresh rate of the modulation index) and the equivalent delay implied on the maintenance of the PWM index (one-half the PWM index refresh rate). All other "hardware" time delays take lower impact while uncertain and equivalent for all control cases.

1st Case (DSP1): 1 sample - 1 refresh / PWM period.

The basic DSP control algorithm adopts the current sample i_{k-1} acquired on the t_{k-1} instant in order to generate the modulation index value D_k, which is maintained for the next whole PWM period (comprised between t_k and t_{k+1}).

$$D_k = Alg(I^*_{k-1}, i_{k-1}) \tag{1}$$

2nd Case: 2 averaged samples - 1 refresh / PWM period.

In order to improve the measurement accuracy, that is reducing the sensitivity to PWM ripple and noise, it is possible to better evaluate the current mean value by averaging two consecutive current samples.

With reference to Fig. 5 sketch, the samples acquired on the instants t_{k-1} and $t_{k-1/2}$ are averaged to refresh the modulation index D_k at the time t_k. The total A/D input to S/H refresh time-delay can be equivalently associated to an ideal feedback sample kept at the instant $t_{k-3/4}$.

The "freshest" reference value is related to the last of the two feedback samples.

$$D_k = Alg(I^*_{k-1/2}, \tilde{i}_{k-3/4}) \;;\; \tilde{i}_{k-3/4} = \frac{i_{k-1} + i_{k-1/2}}{2} \tag{2}$$

3rd Case (DSP2): 2 averaged samples - 2 refreshes / PWM period.

The closed-loop bandwidth can be increased by doubling the algorithm execution rate, holding the PWM error rejection as in 2nd case. The modulation index is refreshed twice, that is on both positive and negative carrier peaks:

$$D_{k-1/2} = Alg(I^*_{k-1}, \tilde{i}_{k-5/4}) \;;\; \tilde{i}_{k-5/4} = \frac{i_{k-3/2} + i_{k-1}}{2} \tag{3}$$

$$D_k = Alg(I^*_{k-1/2}, \tilde{i}_{k-3/4}) \;;\; \tilde{i}_{k-3/4} = \frac{i_{k-1} + i_{k-1/2}}{2} \tag{4}$$

4th Case: 2 samples - 2 refreshes / PWM period.

From theoretical point of view, the best dynamic performances are reached by double index refreshment and not averaged sampled feedback.

This is analytically expressed by the following equations:

$$D_{k-1/2} = Alg(I^*_{k-1}, i_{k-1}) \tag{5}$$

$$D_k = Alg(I^*_{k-1/2}, i_{k-1/2}) \tag{6}$$

III.C. Comparison of sampled control techniques.

The four cases defined above are easily compared in terms of time-delays, as reported in Table 1. On the opposite, their sensitivity to PWM ripple and noise can be only qualitatively defined.

TABLE I COMPARATIVE SUMMARY OF DSPs' PERFORMANCES

	1st Case (DSP1)	2nd Case	3rd Case (DSP2)	4th Case
PWM triangular ripple rejection	LOW	GOOD	GOOD	critical
H.F. rejection	Analog filter			
A/D to S/H delay	T_{sw}	$3/4T_{sw}$	$3/4T_{sw}$	$1/2T_{sw}$
A/D to PWM delay	$3/2T_{sw}$	$5/4T_{sw}$	T_{sw}	$3/4T_{sw}$

The fourth case is somewhat the peculiar one, since it is hardly affected by particular limit cycle at fundamental PWM frequency. This limit cycle arises due to the PWM ripple sensitivity amplified by high loop-gain values, since at the limit cycle operation the zero-crossing instants of the PWM current ripple are counter-displaced to each other in two adjacent halves of the PWM period.

In Fig. 6 the steady-state behaviour of the modulation index is reported for the 3rd and 4th cases, showing for the latter the limit cycle superimposed to controlled mean value. The dramatical effect of averaged feedback samples in the 3rd case avoids any limit cycle sensitivity.

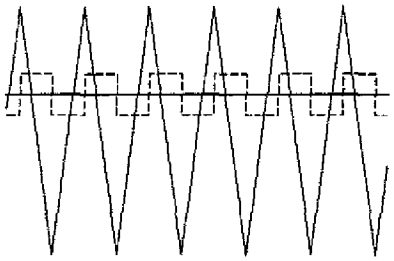

Fig. 6 Steady-state behaviour of DSP control loops by 2 samples and 2 refreshes for PWM modulation: 3rd case (continuos line), 4th case (dashed line).

For the same cases, their rejection to digital white noise superimposed to input A/D signal is reported in Fig. 7. The averaging properties are pointed-out also in this test, indicating that a "quieter" closed-loop behaviour is achieved in noisy environment.

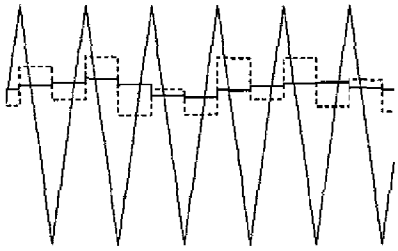

Fig. 7 Rejection to white noise in the same cases reported in Fig. 6.

IV. Top-Performance Digital FPGA-based PWM Control Loop

IV.A. Breakthrough concept: ideal PWM filter.

In a DSP-based PWM control loop, the minimum delay between the last sampling instant and the next index refresh is $T_{sw}/2$, even if the computation time could be lower than.

This constraint can be overcame by the adoption of an alternative current measurement technique, where the sampling instants can be freely positioned with respect to the PWM carrier vertexes. On the other hand, a really free samples positioning must be realised without increasing the sensitivity to PWM errors.

The only way is to measure directly the mean value of the current feedback, which in turn provides the ideal rejection to any possible PWM effect.

This is the ideal PWM filter, whose continuous output, that is the mean value-time variable of the current, can be defined by (7):

$$\tilde{i}(t)=\frac{1}{T_{ripple}}\cdot\int_{t-T_{ripple}}^{t} i(\xi)\cdot d\xi \qquad (7)$$

IV.B. Analysis of the ideal PWM filter.

The Laplace transfer function of the ideal PWM filter in (7) is formulated as follows:

$$AVG\left(sT_{ripple}\right)=\frac{1-e^{-sT_{ripple}}}{sT_{ripple}} \qquad (8)$$

The Bode diagrams of this ideal PWM filter are shown in Fig. 8. This transfer function equals that of the zero-order-hold, where the maintenance time equals the PWM ripple period.

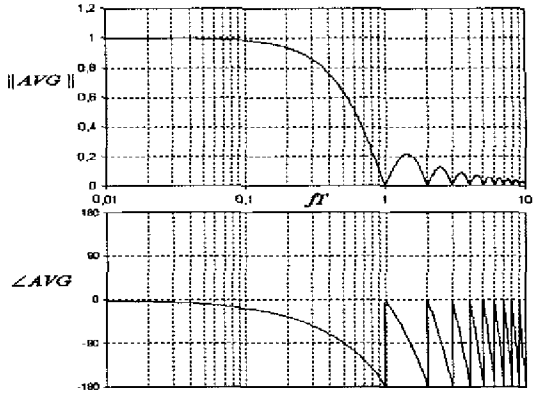

Fig. 8 Ideal PWM filter f.d.r: magnitude and phase Bode diagrams

All PWM harmonics are cancelled. Moreover the global behaviour is like a "low-pass" filter, rejecting both external noise and load resonant effects in response to switchings.

The phase delay is proportional to the frequency and the equivalent time delay results:

$$\Delta t_{PWM,filter}=T_{ripple}/2 \qquad (9)$$

IV.C. A FPGA-based realisation of PWM filter.

The digital implementation of the ideal PWM filter requires an over-sampling strategy in order to realise a discrete calculus of (7): a sufficient number of samples must be chosen depending on the required accuracy.

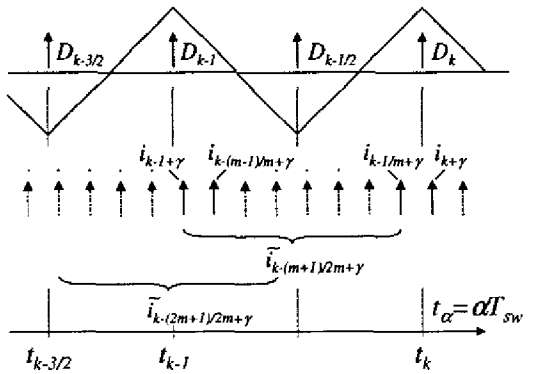

Fig. 9 Sampling and filtering for FPGA control techniques

With reference to Fig. 9 the averaged current value can be expressed as in (10):

$$\tilde{i}_{k-(m+1)/2m} = \frac{1}{m}\sum_{j=0}^{m-1} i_{k-1+j/m} \tag{10}$$

Similarly to the previous description, it's possible to define a new discrete averaging operator, whose L-transform is reported in (11):

$$AVG_m(s) = \frac{1}{m}\cdot\sum_{k=0}^{m-1} e^{-sTk/m} \tag{11}$$

In Fig. 10 the Bode diagrams of AVG_m are reported for m=8. It can be noted the unitary magnitude and the zero phase delay for $fT=8$, this is why the filtering action is null at all the frequencies multiple of m/T. This fact highlights the correlation between a proper m choice and the maximum peak ripple value. As an example, for the reference structure in Fig. 2 the maximum possible error for the mean current estimation results:

$$\left(\delta\Delta i_{L,pk}\right)_{MAX} = \frac{\left(\Delta i_{L,pk}\right)_{MAX}}{m^2} \tag{12}$$

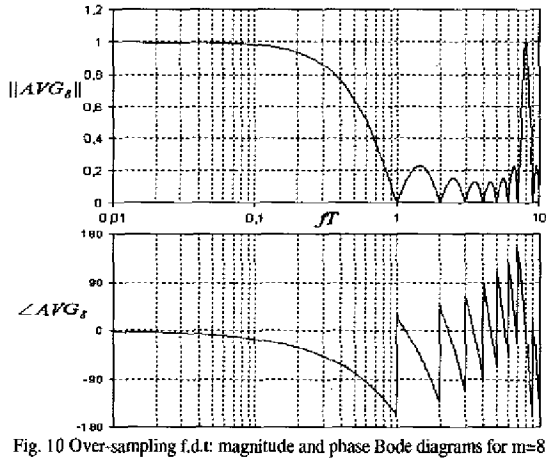

Fig. 10 Over-sampling f.d.t: magnitude and phase Bode diagrams for m=8

The discrete PWM ripple implementation can be completed by adopting an analog filter applied to the current signal. Several criteria can be adopted, dependently on control performance or on high frequency rejection requirements.

An example is reported in Fig. 11, where AVG_8 is compensated by a triple-pole filter, properly chosen in order to set 180° phase delay at $fT=1$:

$$AVG_{8,filtered} = AVG_8(s)\cdot\frac{1}{\left(1+s\tau_{filter}\right)^3} \tag{13}$$

Thanks to this improvement, the discrete PWM filter $AVG_{8,filtered}$ is practically equal to the ideal one up to $fT=4$.

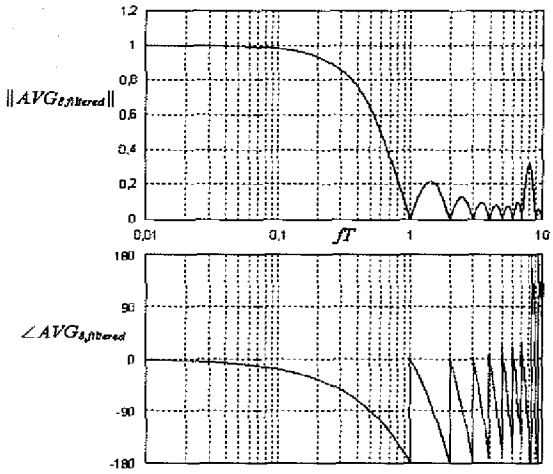

Fig. 11 Over-sampling +external analog filter f.d.t: magnitude and phase Bode diagrams for m=8

IV.D. Single and double index refresh

The ideal PWM ripple filter can be implemented in a PLD device. Moreover, thanks to the capability and versatility of the latest FPGAs, it's possible to implement all the control functions into a single chip.

Considering PWM converters for medium-high power applications, the switching frequency is around 5kHz÷20kHz and the control tasks implemented in a FPGA require a little percentage of T_{sw}. This means that the computation time can be disregarded, so the total loop delay can be minimised down to the sum between the PWM ripple filter delay and the index maintenance time delay.

1st Case (FPGA1): PWM filter - 1 refresh / PWM period.

Considering a single index refresh per PWM period, the index computation dependence is expressed by the following:

$$D_k = Alg(I_k^*, \tilde{i}_{k-1/2}) \tag{14}$$

2nd Case (FPGA2): PWM filter - 2 refresh / PWM period.

Doubling the index refresh frequency the index computation is formally expressed by the followings:

$$D_{k-1/2} = Alg(I_{k-1/2}^*, \tilde{i}_{k-1}) \tag{15}$$

$$D_k = Alg(I_k^*, \tilde{i}_{k-1/2}) \tag{16}$$

V. Comparative Results

V.A. Overall performances comparison.

In Table 2 the comparative aspects for all the previous analysed cases are quantified. It can be noted that FPGA solutions result better or equivalent in any comparative term.

The PWM ripple and high frequency rejection result strongly improved by the over-sampling technique, assuring robust regulation immunity to the non-idealities. Moreover, thanks to the parallel processing, the very low computation time of FPGAs allows higher dynamic performances as expressed by the total loop delays, since in practice $\Delta t_{calc} << \Delta t_{filter}$.

TABLE 2 COMPARATIVE SUMMARY OF DSPS & FPGAS' PERFORMANCES

	DSP1	DSP2	FPGA1	FPGA2
PWM ripple rejection	LOW	GOOD	VERY HIGH	
High Freq. rejection	Analog filter		YES (Fig. 11)	
Ideal loop delay T_{del}	$3/2T_{sw}$	T_{sw}	T_{sw}	$3/4T_{sw}$
Further real delay	$\Delta t_{PWM}+\Delta t_{filter}$	$\Delta t_{PWM}+\Delta t_{filter}$	$\Delta t_{PWM}+\Delta t_{calc}$	$\Delta t_{PWM}+\Delta t_{calc}$

V.B. Comparison of dynamic behaviour.

The different dynamic performances can be experienced in terms of closed-loop reference step responses. At first a maximum gain criterion is applied to the proportional gain. Then the dead-beat control is realised giving perfect evidence to the different dynamic properties.

Both the current and the PWM index waveforms are reported in Fig. 12 showing the step response: K_P is set in each case to hold the closed-loop damping factor (45° at cross-over frequency); no integrative regulation is here adopted ($\Delta V_{w\text{-}up}=0$).

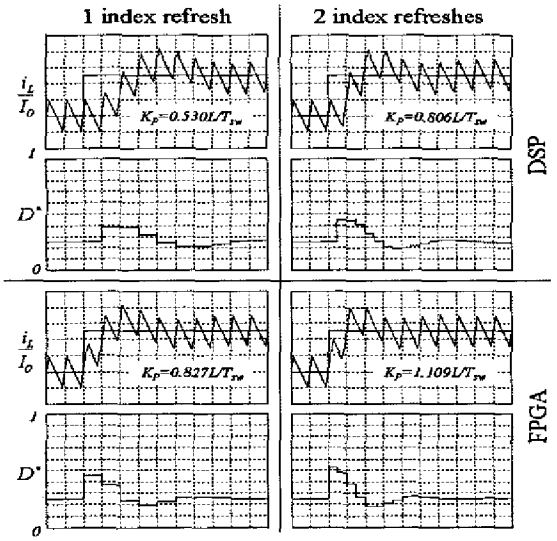

Fig. 12 Closed loop step response with proportional only regulator; $I_0=V_CT_{sw}/L$; $E_f/V_C=0.25$; all p.u. variables (*0.1/div*).

As a consequence of the total loop delay, the case DSP1 have the slowest response; on the opposite, the FPGA2 one is characterised by the best control performance. For the same reason, since the loop delays of the DSP2 and the FPGA1 cases are equal, their responses are very close to each other.

A dead-beat control concept is applied, according to Fig. 3 control structure, to the control loops reported in Fig 12.

The resulting responses are reported in Fig. 13, pointing out the different position and width of the single time slot theoretically needed to get the target.

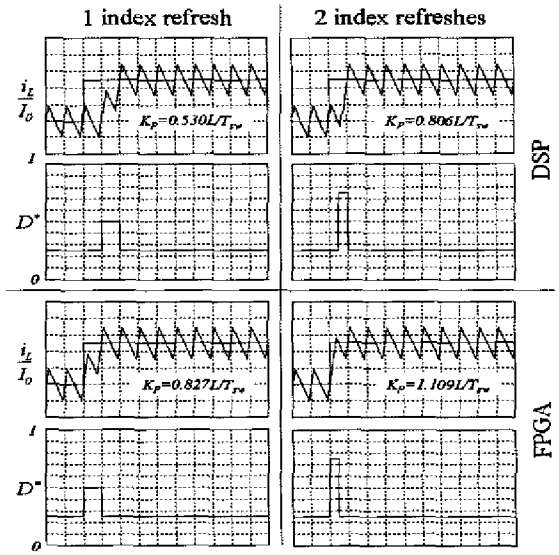

Fig. 13 Dead-beat applied to the same conditions as in Fig. 12.

VI. CONCLUSIONS

A comparison between DSP and FPGA-based control capabilities in PWM power converters has been carried out.

The digital control sensitivity to sampling and control non-idealities has been discussed. The possible over-sampling strategies have been proposed improving PWM ripple and high frequency rejection.

A comparative dynamic performance analysis has been presented in terms of total closed-loop time delay.

The proposed concepts have been applied showing the dynamic response capabilities and pointing out the respective properties in dead-beat control.

It has been demonstrated how FPGA-based digital control properties are better than DSP ones for any comparative term.

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